PCMCIA 2.1 Compliant Industrial FLASH Memory Cards
4 to 32 Megabyte Card Features AMD 16Mbit Compatible Devices
5 Volts Only Operation

Description

These FMJ Storage products are high quality PCMCIA 2.1 compliant Type II FLASH memory cards which operate in a 5 Volt only environment. These cards feature an array of 2 to 20 AMD® Am29F016 16 Megabit FLASH components which are packaged in a quality PCMCIA housing by our ISO 9001 certified production team. FLASH technology assures data retention without the need for battery back-up of any kind, even when system power is removed.

Data may be handled in either 8 bit or 16 bit bus modes. These features make FMJ Storage memory cards especially desirable for a wide variety of custom applications that utilize PCMCIA slots such as PDAs and other handheld devices.

Features

- PCMCIA 2.1 compliant
- FLASH Architecture, non volatile memory
- Single Supply Voltage Operation (5V ±5%)
- Standard 150 ns Access Time from Standby
- Byte-wide and Word-wide access
- Embedded Program/Erase Algorithms
- Erase Suspend/Resume Feature
- 64 Kilobyte Sector Erase Resolution
- High Write Endurance
  100,000 Write/Erase Cycles Min per sector.
- WP Switch to Prevent Accidental Data Loss
- Dedicated Attribute Memory EE PROM
- TYPE II PCMIA Form factor

- ISO 9001 Quality Controls

PIN DESCRIPTION

Signal	Name	Function
A[25:0]	Address Bus	Address Inputs, A25-A0
D[15:0]	Data Bus	Data Input/Outputs
/OE	Output Enable	Active Low for Read
/WE	Write Enable	Active Low for Write
/CE1	Card Enable Low Byte	Active Low for Read/ Write Even Byte
/CE2	Card Enable High Byte	Active Low for Read/ Write Odd Byte
/REG	Register Select	Active Low to enables Attribute Memory
WP	Write Protect	Output Signal indicates the WP switch state
/VS1, /VS2	Voltage Sense 1, 2	Voltage Sense Outputs (both open = 5V card)
/CD1, /CD2	Card Detect Signals 1, 2	Tied to GND
V_{CC}	Power Supply	Power Supply Voltage, +5.0V ±5%
GND (V_{SS})	Ground	Card Ground

PIN ASSIGNMENTS

Pin #	Signal	I/O	Function		Pin #	Signal	I/O	Function	
1	GND		Ground		35	GND		Ground	
2	D3	I/O	Data Bit 3	PL	36	/CD1	O	Card Detect - Grounded	
3	D4	I/O	Data Bit 4	PL	37	D11	I/O	Data Bit 11	PL
4	D5	I/O	Data Bit 5	PL	38	D12	I/O	Data Bit 12	PL
5	D6	I/O	Data Bit 6	PL	39	D13	I/O	Data Bit 13	PL
6	D7	I/O	Data Bit 7	PL	40	D14	I/O	Data Bit 14	PL
7	/CE1	I	Card Enable Low byte	PH	41	D15	I/O	Data Bit 15	PL
8	A10	I	Address Bit 10		42	/CE2	I	Card Enable High byte	PH
9	/OE	I	Output Enable	PH	43	/VS1		Vltg Sense Signal 1- Open	
10	A11	I	Address Bit 11		44	*RFU*		*Reserved For Future Use*	NC
11	A9	I	Address Bit 9		45	*RFU*		*Reserved For Future Use*	NC
12	A8	I	Address Bit 8		46	A17	I	Address Bit 17	
13	A13	I	Address Bit 13		47	A18	I	Address Bit 18	
14	A14	I	Address Bit 14		48	A19	I	Address Bit 19	
15	/WE	I	Write Enable	PH	49	A20	I	Address Bit 20	
16	/BUSY	O	Ready Busy Signal	NC	50	A21	I	Address Bit 21	
17	V_{CC}		Power Supply		51	V_{CC}		Power Supply	
18	*Vpp1*		*Program Voltage 1*	NC	52	*Vpp2*		*Program Voltage 2*	NC
19	A16	I	Address Bit 16		53	A22	I	Address Bit 22 **(Note 1)**	PL
20	A15	I	Address Bit 15		54	A23	I	Address Bit 23 **(Note 1)**	PL
21	A12	I	Address Bit 12		55	A24	I	Address Bit 24 **(Note 1)**	PL
22	A7	I	Address Bit 7		56	A25	I	Address Bit 25	NC
23	A6	I	Address Bit 6		57	/VS2		Vltg Sense Signal 2- Open	
24	A5	I	Address Bit 5		58	RESET	I	Hardware RESET	NC
25	A4	I	Address Bit 4		59	WAIT	O	Wait State Control **(Note 2)**	NC
26	A3	I	Address Bit 3		60	*RFU*		*Reserved For Future Use*	NC
27	A2	I	Address Bit 2		61	/REG	I	Register Select	PH
28	A1	I	Address Bit 1		62	/BVD2	O	Batt. Voltage Detect 2	PH
29	A0	I	Address Bit 0	PL	63	/BVD1	O	Batt. Voltage Detect 1	PH
30	D0	I/O	Data Bit 0	PL	64	D8	I/O	Data Bit 8	PL
31	D1	I/O	Data Bit 1	PL	65	D9	I/O	Data Bit 9	PL
32	D2	I/O	Data Bit 2	PL	66	D10	I/O	Data Bit 10	PL
33	WP	O	Write Protect		67	/CD2	O	Card Detect - Grounded	
34	GND		Ground		68	GND		Ground	

Notes:

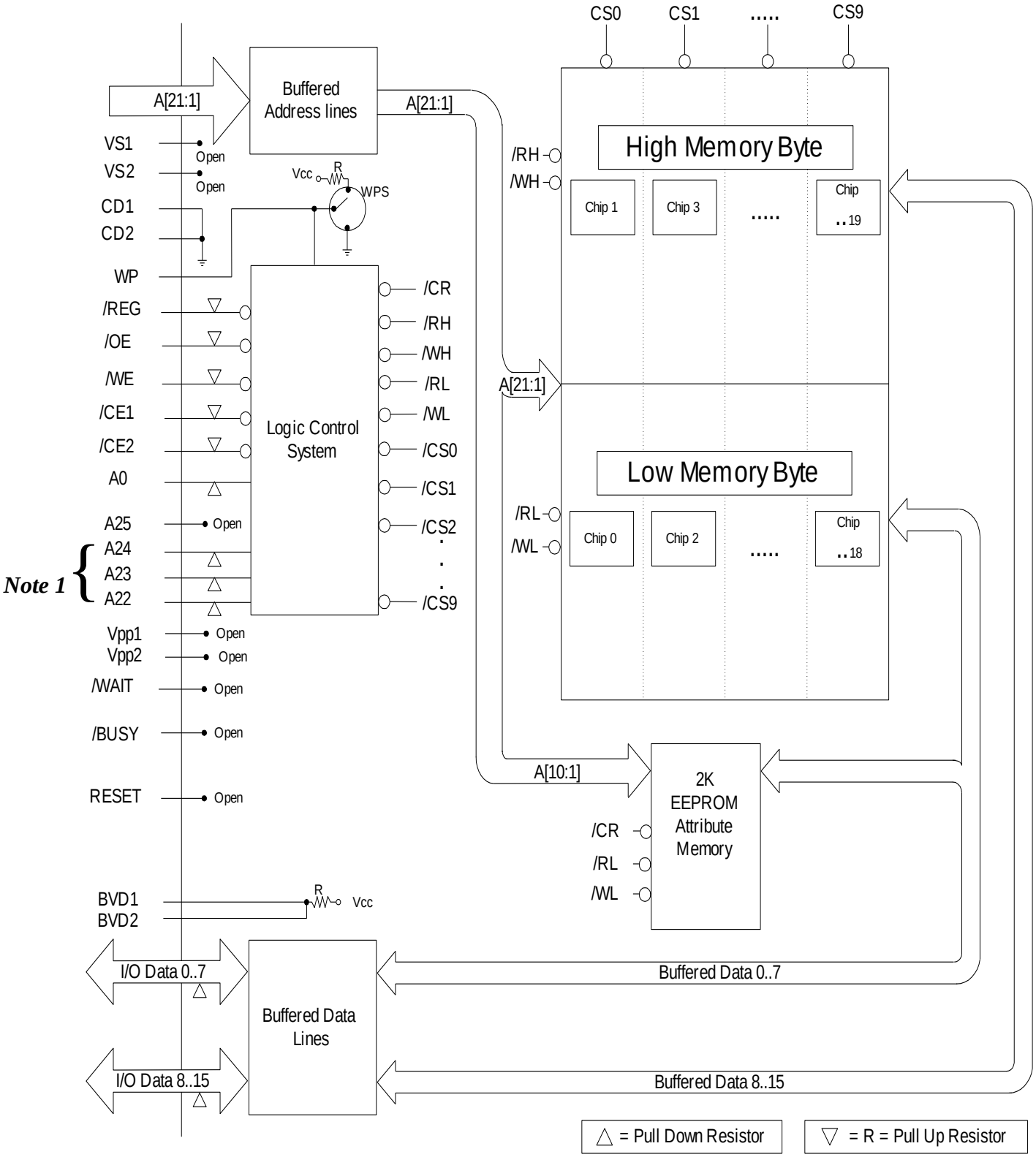
1. *Upper Address Lines are decoded.*
2. *There are not wait states generated by these cards. This Signal must be pulled by the Host socket.*

Legend:

I = *Input to card only*
O = *Output from card only*
I/O = *Bi-directional signal*
PH = *Pulled High (10 - 50K Typ.)*
PL = *Pulled Low (100K Min.)*
NC = *Not Connected*

Functions of the shaded pins are not used.

FUNCTIONAL BLOCK DIAGRAM



Note

1. *Upper address lines are decoded.*

COMMON MEMORY BUS OPERATIONS

Operation	/REG	/CE2	/CE1	/OE	/WE	A0	D8-D15	D0-D7
READ								
Read Even (x8)	H	H	L	L	H	L	High -Z	**Data Out-Even**
Read Odd (x8) **(Note 1)**	H	H	L	L	H	H	High -Z	**Data Out-Odd**
Read Odd (x8)	H	L	H	L	H	X	**Data Out-Odd**	High-Z
Read Word (x16)	H	L	L	L	H	X	**Data Out-Odd**	**Data Out-Even**
WRITE/ERASE								
Write Even (x8)	H	H	L	H	L	L	High -Z	**Data In-Even**
Write Odd (x8) **(Note 1)**	H	H	L	H	L	H	High -Z	**Data In-Odd**
Write Odd (x8)	H	L	H	H	L	X	**Data In-Odd**	High-Z
Write Word (x16) **(Note 2)**	H	L	L	H	L	X	**Data In-Odd**	**Data In-Even**
INACTIVE								
Card Output Disable	X	X	X	H	X	X	High-Z	High-Z
Standby	X	H	H	X	X	X	High-Z	High-Z

Notes:

1. *Byte access - Odd. In this x8 mode, A0 = V_{IH} outputs or inputs the "odd" byte (high byte of the x16 word on D0 - D7). This is accomplished internal to the card by transposing D8-D15 to D0-D7.*
2. *During 16-bit write and erase operations one IC of a device pair may complete the operation prior to the other. It is therefore necessary to monitor the card busy signal or poll both components before considering the operation complete.*

Legend:

H = V_{IH}
L = V_{IL}
X = Don't Care

Warning: The raising of address lines to voltages levels above CMOS levels is not permitted. Applying voltages above these levels will destroy the card. Any attempt to identify memory components in this way is not permitted.

ATTRIBUTE MEMORY BUS OPERATIONS

Pins/Operation	/REG	/CE2	/CE1	/OE	/WE	A0	D8-D15	D0-D7
READ (Note 1)								
Read Even (x8)	L	H	L	L	H	L	High -Z	**Data Out-Even**
Read Odd (x8) **(Note 2)**	L	H	L	L	H	H	High -Z	Data Out-Odd Not Valid
Read Odd (x8) **(Note 2)**	L	L	H	L	H	X	Data Out-Odd Not Valid	High-Z
Read Word (x16) **(Note 2)**	L	L	L	L	H	X	Data Out-Odd Not Valid	**Data Out-Even**
WRITE (Note 1)								
Write Even (x8)	L	H	L	H	L	L	High -Z	**Data In-Even**
Write Odd (x8) **(Note 3)**	L	H	L	H	L	H	High -Z	Data In-Odd Not Valid
Write Odd (x8) **(Note 3)**	L	L	H	H	L	X	Data In-Odd Not Valid	High-Z
Write Word (x16) **(Note 3)**	L	L	L	H	L	X	Data In-Odd Not Valid	**Data In-Even**
INACTIVE								
Card Output Disable	X	X	X	H	X	X	High-Z	High-Z
Standby	X	H	H	X	X	X	High-Z	High-Z

Note:

1. *Refer to the data sheets for the Microchip 28C16A EEPROM for details on programming the attribute memory.*
2. *Data Read operations will produce data information that has no valid meaning for the Odd byte of information.*
3. *Data Write operations may be initiated, however data information for the Odd byte will not be stored.*

Legend:

H = V_{IH}
L = V_{IL}
X = Don't Care

Warning: The raising of address lines to voltages levels above CMOS levels is not permitted. Applying voltages above these levels will destroy the card. Any attempt to identify memory components in this way is not permitted.

PIN DESCRIPTIONS

Vcc
Card Power Supply

Power input required for device operation. The Vcc must be 5.0 V ± 5% (4.75V to 5.25V).

GND
Card Ground

The VSS pins of all IC components and related circuitry are connected to this card ground, which must be connected to the Host systems ground.

NC
Not Connected

These pins are physically not connected to any circuitry.

A0-A25
Address Bus

These signals are address input lines that are used for accesses to card memory. A0 is used to select the odd or even bank of memory components. A22 through A24 select which Device Pair of ICs will be accessed. A1 through A21 are used to select the specific address that is to be accessed on an individual memory component. Address A25 is Not Connected.

D0-D15
Data (Input/Output) Bus

Data lines D0 through D15 are used to transfer data to and from the card. When memory is not selected or outputs are disabled data lines are placed in a high impedance state.

/OE
Output Enable Signal

This active low input signal enables memory devices to activate data lines and output data information.

/WE
Write Enable Signal

This active low input signal controls memory write functions and is used to strobe data into the card memory.

WP
Write Protect Signal

This output signal indicates whether or not card write operations have been disabled by the Write Protect Switch (WPS). When the signal is asserted high, card-write operations are disabled. When this signal is asserted low, the card-write operations will function normally.

/CE1, /CE2
Card Enable

These are active low inputs used to enable the card memory. /CE1 accesses the low bank of memory which provides storage for even numbered bytes. /CE2 accesses the high bank of memory which provides storage for odd numbered bytes. During byte-wide operations these Card Enable signals are used in conjunction with address line A0 to access even or odd bytes of data. The memory card is de-selected and power consumption is reduced to stand-by levels when both /CE1 and /CE2 are driven high.

PIN DESCRIPTIONS *(CONTINUED)*

/REG
Register Select Signal

This active low input signal enables access to the Attribute memory EEPROM. Attribute memory is typically used to store the CIS file, which contains specific card information. Access to common memory is not possible when /REG is asserted low.

RESET
RESET Signal

This is an active high input signal that normally is used by the Host to place the card in the deep power down mode of operation. On these cards this signal is Not Connected.

/WAIT
Extended Bus Cycle

This active low output signal is used by the card to delay completion of a memory access operation. There are no wait states generated by these memory cards. For this reason the /WAIT signal is left open. It is the responsibility of the Host to pull this signal high to prevent false activation.

/BUSY
Ready Busy Signal

This active low output signal normally indicates that at least one memory device in the card is busy performing a task. On these cards this signal is Not Connected.

/CD1, /CD2
Card Detect

These pins are tied directly to ground and are used by the Host system to detect the presence of the card. If /CD1 and /CD2 are not both detected low by the Host, then the card is not properly inserted.

/VS1, /VS2
Voltage Sense Signals

The Voltage Sense Signals notify the socket of the card's Vcc requirements on initial power up. When both /VS1 and /VS2 are open, as is the case on these cards, the card is identified to the Host system as a 5V only card.

/Vpp1, /Vpp2
Program and Peripheral Voltages

These signals are normally used to supply additional programming voltages for memory devices that require programming voltages other than the Vcc supply. This memory card requires Vcc voltages only. Therefore Vpp1 and Vpp2 are Not Connected.

/BVD1, /BVD2
Battery Voltage Detect

These pins are normally used to indicate the status of an internal card battery. Since FLASH cards do not require or use a battery, these signals are internally pulled high by a resistor.

MANUFACTURER'S IDENTIFICATION CODE TABLE

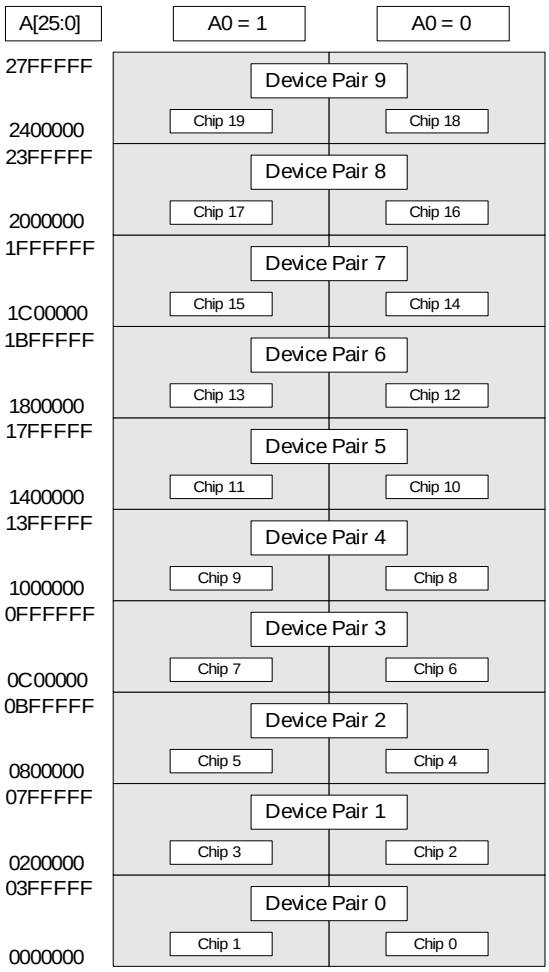
Device	Manufacturer	Hex Data		Operational Voltages
		Manufacturer Code	Device Code	V_{CC}
Am29F016 /Compatible	AMD Compatible	01h	ADh	5V ± 5%

The component manufacturer and device ID codes of each common memory component may be read from the Card Information Structure (CIS), or directly from each memory device. The CIS file is located in the Attribute Section of the card memory. Typically the CIS is stored in the EEPROM.

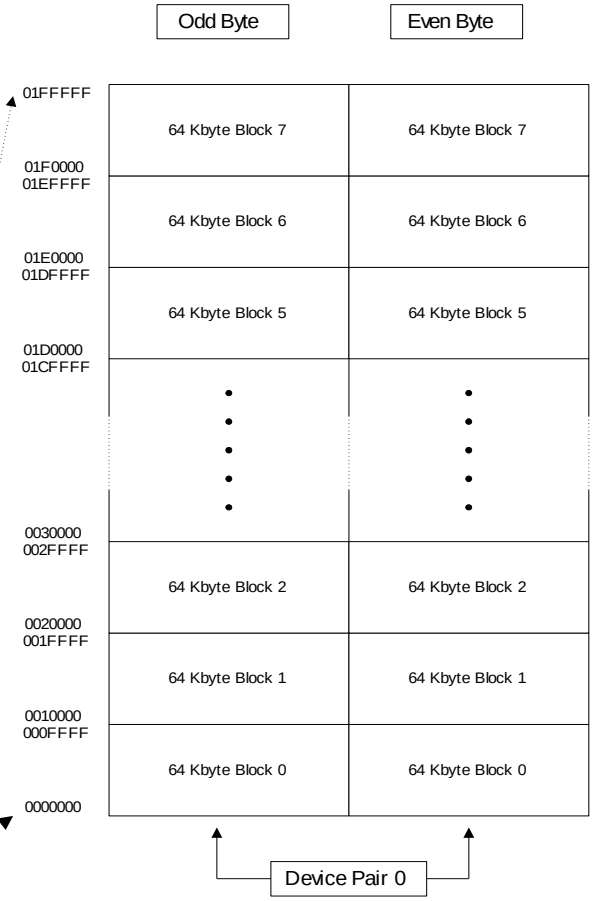
Directly reading the IDs from a memory component may be done by initiating the embedded Autoselect Command (See COMMAND DEFINITIONS Table for command sequence and codes). Once the appropriate command sequence codes have been written to a device, a read operation at chip address 00000h will return the Manufacture ID code and a read at 00001h will return the device ID code for the specific component use on the Card. This mode may only be exited by initiating valid read command operation.

For complete details of these memory devices refer to the manufacturers published data sheets.

CARD COMMON MEMORY MAP

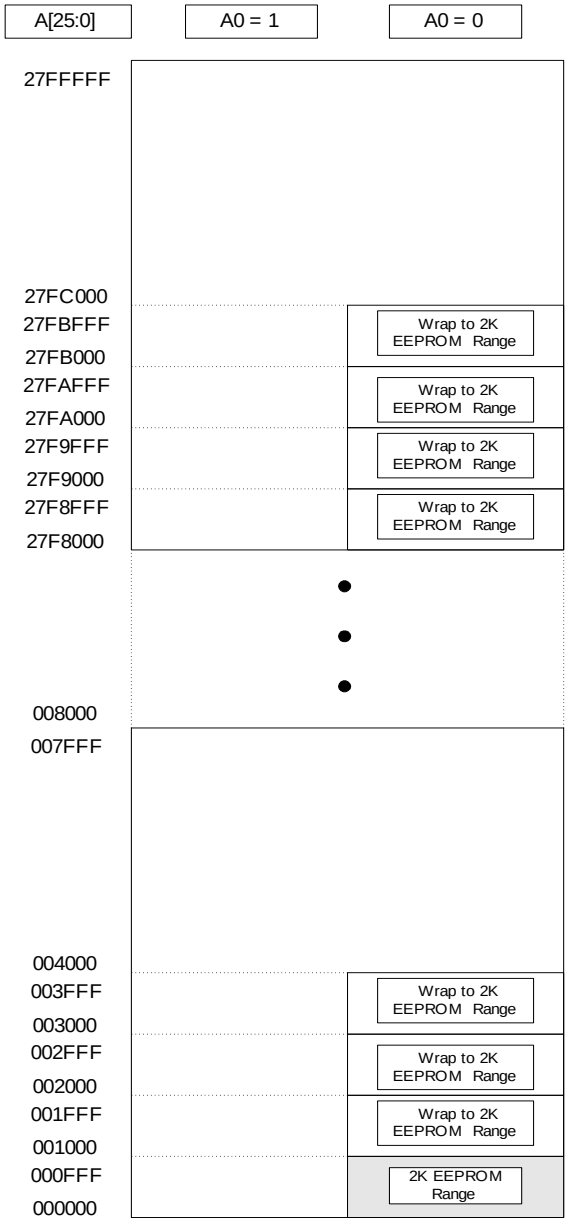


Each Device Pair Represents 4MByte of Card memory.

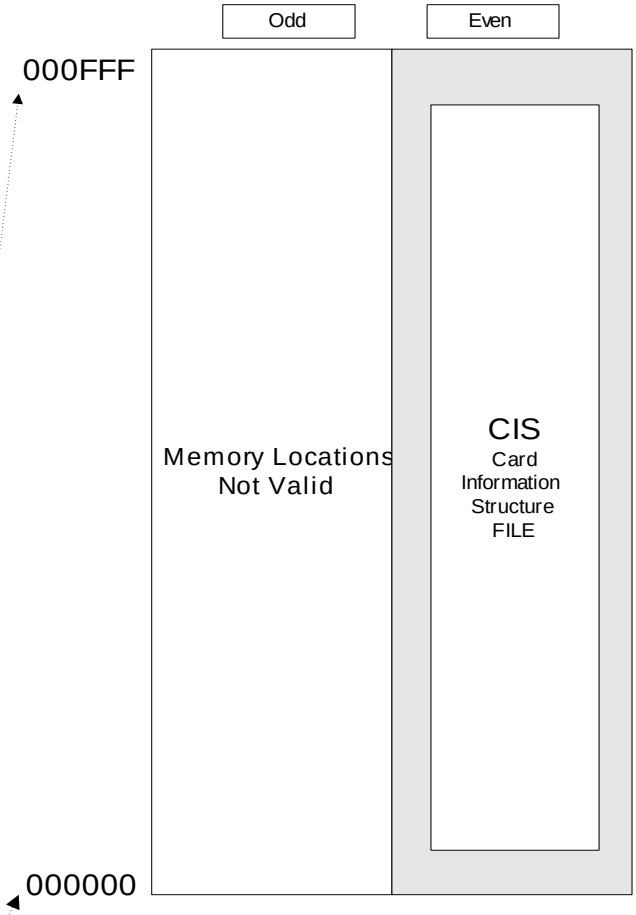


Each 16bit memory chip is segmented into 16 equally spaced 64 Kbyte blocks

ATTRIBUTE MEMORY MAP



The CIS file is located only in even bytes of the card memory.



Attribute Memory Wrap around addressing occurs at every 2K increments.
The EEPROM is deactivated, whenever A14 = 1.

Addresses above 008000h wrap around to the same location as 000000h at every 32K intervals.

COMMAND DEFINITIONS TABLE

All Address and Data values are in Hexadecimal unless otherwise noted. Addresses (Addr) are chip ,not card, addresses.

Embedded Command Sequence	Bus Cyc.	1st Bus Write Cycle			2nd Bus Write Cycle			3rd Bus Write Cycle			4th Bus Write Cycle			5th Bus Write Cycle			6th Bus Write Cycle		
		Addr	Data		Addr	Data		Addr	Data		Addr	Data		Addr	Data		Addr	Data	
			Evn	Odd		Evn	Odd		Evn	Odd		Evn	Odd		Evn	Odd		Evn	Odd
Read/Reset	1*	XXXX	F0	F0															
Read/Reset	4	5555	AA	AA	2AAA	55	55	5555	F0	F0	RA	RH	RL						
Autoselect Manf. ID	4	5555	AA	AA	2AAA	55	55	5555	90	90	XX00	01	01						
Autoselect device ID	4	5555	AA	AA	2AAA	55	55	5555	90	90	XX01	AD	AD						
Word Write	4	5555	AA	AA	2AAA	55	55	5555	A0	A0	PA	PH	PL						
Device Erase	6	5555	AA	AA	2AAA	55	55	5555	80	80	5555	AA	AA	2AAA	55	55	5555	10	10
Sector Erase	6	5555	AA	AA	2AAA	55	55	5555	80	80	5555	AA	AA	2AAA	55	55	SA	30	30
Sector Erase Suspend		XXXX	B0	B0	Erase can be suspended during sector erase with Addr (don't care), Data (B0B0h)														
Sector Erase Resume		XXXX	30	30	Erase can be resumed after suspend with Addr (don't care), Data (3030h)														

Note:

* *Operation available after a card power reset, or after write/erase operations have completed.*

Write protect must not be enabled for proper command operations. Address bits A19-A11 are Don't Care for all commands except for Read Address (RA), Program Address (PA), and Sector Address (SA). For any word operation both the Even and Odd byte device must be made active through the control line settings. Refer to the Memory Bus Operations Table for control line settings for various operation modes.

Legend:

X = any valid address with in a memory device

It should be noted that addresses are latched on the falling edge of the /WE pulse and that data is latched on the rising edge of /WE (See CARD TIMING CHARACTERISTICS).

CARD ADDRESS VS CHIP ADDRESS CALCULATIONS

Specific memory addresses may be calculated by the following method;

Card Address	Chip Address	Device Pair Number	Chip Memory Capacity	Binary Shift Left by 1 bit	A0 = 0 = Even byte A0 = 1 = Odd byte
A [25 : 0] =	(Addr + (DP# *	200000h)	) *	2) +	A0

Where: Addr = Chip addresses.

DP# = the device pair number that the memory device belongs to (see Common Memory Map).

A0 = Card address line used for access to even or odd byte of memory.

COMMAND DEFINITIONS TABLE *(CONTINUED)*

Reset / Read Command:

Cards may be read in Byte wide or Word-Wide modes. In Word-Wide mode, each byte of memory is independently read from each device pair. Each memory device in the card may read at different rates. Therefore the Host should wait until each byte has a valid data output (See MEMORY BUS OPERATIONS Table for specific Control line States and CARD TIMING CHARACTERISTICS for timing information).

Upon power reset of the Card, each memory chip automatically powers up in the Read/Reset state in order to prevent spurious data changes during power up, and does not require an additional Read command in order to begin reading data from memory at this time. This operation mode can also be initiated by writing the Read/Reset Command (See Command Definitions Table). The device remains enabled for read operations until another command is written.

Data reads may also be performed during the Sector Erase Suspend operation. This state is known as the Pseudo Read state. For further details see Sector Erase Suspend and Data Polling.

Standby Mode of Operation:

During any operation only certain memory devices are active. Those that are not involved in a specific operation and are not directly made active by control signals can be placed into a reduced power mode by setting the /CE1 and /CE2 signals to a high logic state. Data output bits are then placed in a high-impedance state independent of /OE. If a device is deselected during block erase, byte write or lock-bit operations, the device continues functioning normally until the operation is completed then enters the Standby Mode (See MEMORY BUS OPERATIONS Table for specific control line states see also CARD DC CHARACTERISTICS for the standby current value).

Each chip may be brought out of standby mode and made active by setting the chip enable signals to a low logic value.

COMMAND DEFINITIONS TABLE *(CONTINUED)*

Embedded Device Erase Command:

Upon executing the Embedded Erase command sequence, the addressed memory device automatically writes and verifies the entire sector(s) for an all "0" data pattern, at which point a self timed chip erase-and-verify begins. The erase and verify operations are complete when the data on D7 (D15 on the odd byte) of the memory device is "1". At which time the device returns to the read mode.

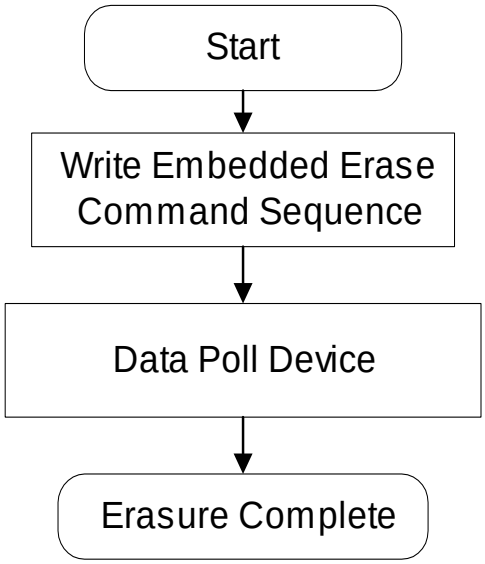
The system is not required to provide any control or timing during these operations. If a power reset occurs while the erase operation is in progress, the erase operation will stop, and the data in that device will be undefined. Note that for the device erase or sector erase operation, Data Polling may be performed at any address in that device or sector (See Polling Operations).

A system designer has the following choices when initiating the Embedded Erase command:

- The Host may keep the sector address valid during the entire Embedded Erase operation.
- Once the system has initiated the Embedded Erase command sequence, the Host may remove the address from the device and perform other tasks. (When the Host comes back to poll the device, it must reassert the same address.)

Embedded Erase Algorithm Description Table and Diagram:

Bus Operations	Command	Comments
Standby		Wait for V_{CC} ramp
Write	Embedded Erase Command sequence	6 Bus Cycle operations
Read		Data Poll to verify completion



COMMAND DEFINITIONS TABLE *(CONTINUED)*

Sector Erase Command:

The sequence of six command codes for executing a Sector Erase may be seen in the COMMAND DEFINITIONS Table. The sector address and the command data are both internally latched on board each memory device. Sector Erase will begin 100µs after the rising edge of the last sector erase command.

During the 100µs time-out period, multiple sectors may be queued for concurrent erase. Queuing of multiple sectors is accomplished by writing the six bus cycle operation commands sequence, followed with writes of the sector erase command 30h to addresses in other sectors desired to be concurrently erased. The system is not required to provide any controls or timing during these operations and any command other than Sector Erase within the time-out window will reset the device to the read mode.

If a power reset occurs after the device has begun executing this command, the erase operation will be halted and the data in the sector will be undefined. The automatic sector erase terminates when the data on D7 (D15 on the odd byte) is "1". Data polling must be performed at an address within any of the sectors being erased.

Sector Erase Suspend/Resume:

Sector Erase Suspend command allows the Host to interrupt the erase operation of the chip and then do data reads (pseudo-read) from a non-busy sector. The chip will take between 0.1µs to 15µs to suspend the erase operation and go into erase suspended read mode.

This mode is only available during the Sector Erase operation and will be ignored during other command operations. Writing this command during the Sector Erase 100µs time-out period will result in immediate suspension of the Sector Erase operation.

Once the device has entered the Sector Erase Suspend mode, any further writes of the command (B0h) at this time will be ignored. Any attempt to initiate other commands during the Erase Suspend mode window will reset the device to read mode. In order to resume the Sector Erase operation, the Resume command (30h) should be written to the suspended device.

Note that the Host system must keep track of what state the chip is in by monitoring D6 (D14 on the odd byte) to determine if a chip has entered the pseudo-read mode (See Polling Operations for Toggle Bit D6).

COMMAND DEFINITIONS TABLE *(CONTINUED)*

Embedded Program Command:

The Embedded Program setup consists of four command codes (See COMMAND DEFINITIONS TABLE). Once the Embedded Program commands are written, the next /WE pulse causes a transition to an active programming operation (See CARD TIMING CHARACTERISTICS). The Host system is not required to provide further control timing the device will automatically provide an adequate internally generated write pulse and verify margin.

When the automatic programming operation is completed, the device returns to the Read mode and the data on D7 (D15 on the odd byte) is equivalent to the data written.

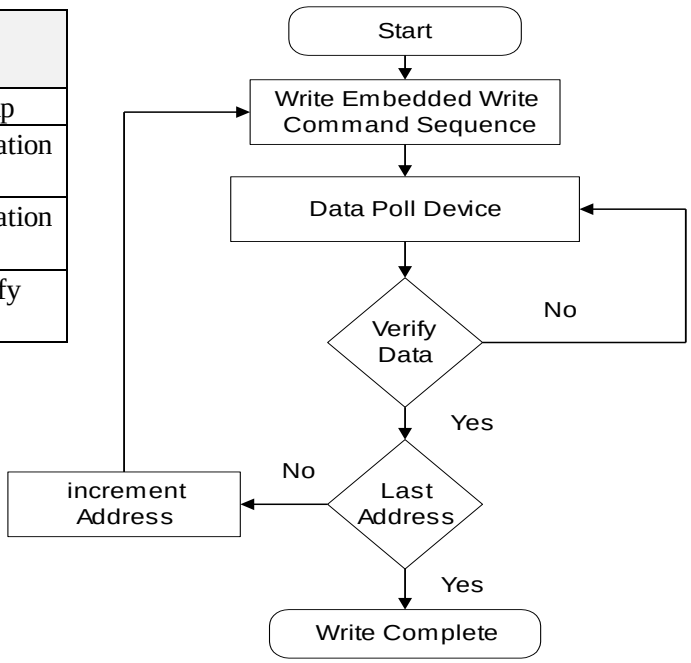
In Word-Wide mode, each byte is independently programmed on each memory device pair. Because each device may reach completion of the programming operation at different times, software polling should continue to monitor each byte for write completion and data verification.

A system designer has the following choices when initiating the Embedded Programming command:

- The Host may keep the address valid during the entire Embedded Programming operation.
- Once the system has initiated the Embedded Program command sequence, the Host may remove the address from the device and perform other tasks. (When the Host comes back to poll the device, it must reassert the same address.)

Embedded Program Algorithm Description Table and Flow Chart:

Bus Operations	Command	Comments
Standby		Wait for V_{cc} ramp
Write	Embedded Program Command sequence	3 bus cycle operation
Write	Program Address/Data	1 bus cycle operation
Read		Data Poll to verify completion



COMMAND DEFINITIONS TABLE *(CONTINUED)*

Polling Operations:

Polling is a method to indicate to the Host system that the Embedded algorithms are either in progress or complete and these is only active during the Embedded Programming or Erase modes of operation.

Data Polling Bit D7 (D15 on the odd byte)

During a embedded programming cycle, any attempt to read from a device will produce the complement of expected valid data on D7. While an embedded erase cycle is being performed, D7 (D15 on the odd byte) will read "0" until the erase is completed. Upon completion of the erase operation the data on D7 (D15 on the odd byte) will read "1".

Even if D7 that the device has completed the embedded operation, the other data bits of the byte D0-D6 may still be invalid since the switching time for each data bit will not be the same. The valid data will be provided only after a certain time delay (> t_{GLQV}) (See CARD TIMING CHARACTERISTICS).

Toggle Bit D6 (D14 on the odd byte)

During an Embedded Program/Erase Algorithm cycle, successive attempts to read (/OE toggling) data from the device at any address will result in D6 (D14 on the odd byte) toggling between logical one and zero. Once the Embedded Program/Erase Algorithm cycle is complete, D6 (D14 on the odd byte) will stop toggling and valid data will be read on the next successive attempt. This bit can also be used in conjunction with toggle bit D2 in order to determine whether the device is in the active erase mode or if that mode has been suspended. (See Command Status Flags Table)

Time Limit Exceeded Bit D5 (D13 on the odd byte)

Time Limit Exceeded indicates a failure of the performed operation, and is identified by the D5 bit set to logical one.

Sector Erase Timer D3 (D12 on the odd byte)

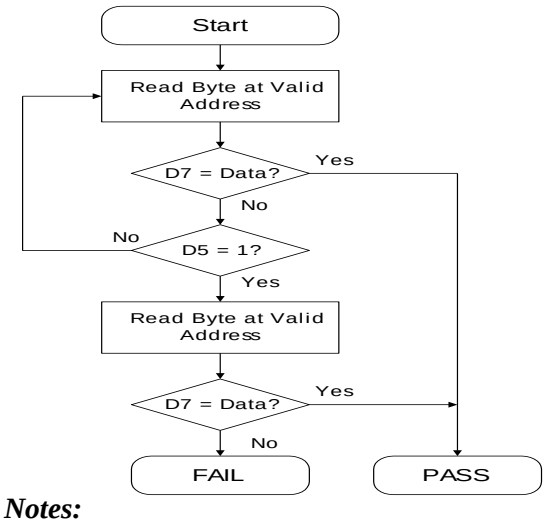
When a sector erase command has been issued a time out window is initiated. This bit is used to indicate whether the sector erase time out period is active or if the window has closed. If D3 (D12 on the odd byte) is a logical one, the internal erase cycle is in progress and the device will not accept additional command inputs. If the D3 bit is logical zero, the time out window is still open and the device will accept additional sector erase commands.

Toggle Bit D2 (D11 on the odd byte)

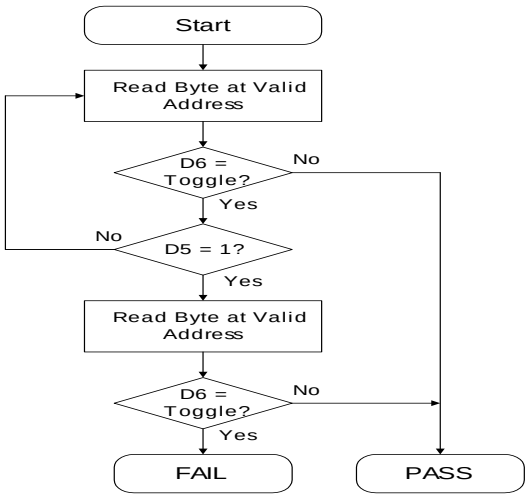
This bit is used in conjunction with toggle bit D6 in order to determine the mode of operation that the internal workings of the memory device are in (See Command Status Flags Table). If the device is involved with an embedded erase or erase suspend command, then the D2 bit (D11 on the odd byte) will be seen to toggle when read successively from an address sector that is being erased. If the device is involved in program operations during an erase suspend period, then the D2 bit will produce a logical one value when read from the address being programmed.

COMMAND DEFINITIONS TABLE *(CONTINUED)*

Data Polling Algorithm:



Toggle Bit Algorithm:



Notes:

1. *D7 is rechecked if D5 = 1 because D7 may change simultaneously with D5.*
2. *D6 is rechecked if D5 = 1 because D7 may change simultaneously with D5*
3. *Bits D7,D6, and D5 correspond to bit D15, D14, and D13 on the odd byte respectively.*

Command Status Flags Table:

Operation (Note 1)	Operation Status	D7	D6	D5	D3	D2
Embedded Program Command (Byte Program)	IP	/D7	Toggle	0	0	1
Embedded Erase Command	IP	0	Toggle	0	1	Toggle
Sector Erase Suspend Read (Pseudo-read) from sector involved in Erase	IP	1	1	0	0	Toggle
Sector Erase Suspend Read (Pseudo-read) from sector not involved in Erase	IP	Data	Data	Data	Data	Data
Sector Erase Suspend Program **(Note 2)** from sector not involved in Erase	IP	/D7	Toggle **(Note 3)**	0	1	1
Embedded Program Command (Byte Program)	TLE **(Note 4)**	/D7	Toggle	1	0	1
Program/Erase Embedded Erase Command	TLE **(Note 4)**	0	Toggle	1	1	N/A
Sector Erase Suspend Program	TLE **(Note 4)**	/D7	Toggle	1	1	N/A

Note:

1. *Data Bits [7:0] corespond to Data bits [15:8] of the High Byte.*
2. *Read operations performed at the address being programmed.*
3. *Performing successive reads from <u>any</u> address will cause D6 to toggle.*
4. *Time Limit Exceeded indicates a failure of the performed operation*

Legend:

IP = Command is In Process
TLE = Time Limits Exceeded
N/A = Address of the memory sector to be erased.

and is identified by the D5 bit.

CARD TIMING CHARACTERISTICS

(Standard operating times for both Common and Attribute Memory unless otherwise noted.)

Read Cycle Timing (/WE = V_{HI})

Parameter	Symbol	Min	Max	Units
Read Cycle Time	t_{AVAV}	150		ns
Address Access Time	t_{AVQV}		150	ns
Card Enable Access Time	t_{ELQV}		150	ns
Output Enable Access Time	t_{GLQV}	100		ns
/OE High to Data Output Disable	t_{GHQZ}		75	ns
/CE Low to Data Output Enable	t_{ELQNZ}	5		ns
Address change to Data no longer valid	t_{AXQX}	0		ns
Address Setup to /OE Low time	t_{AVGL}	20		ns
/OE High Setup to Address time	t_{GHAX}	20		ns
/CE Low Setup to /OE Low time	t_{ELGL}	0		ns
/OE High to /CE High Hold time	t_{GHEH}	20		ns

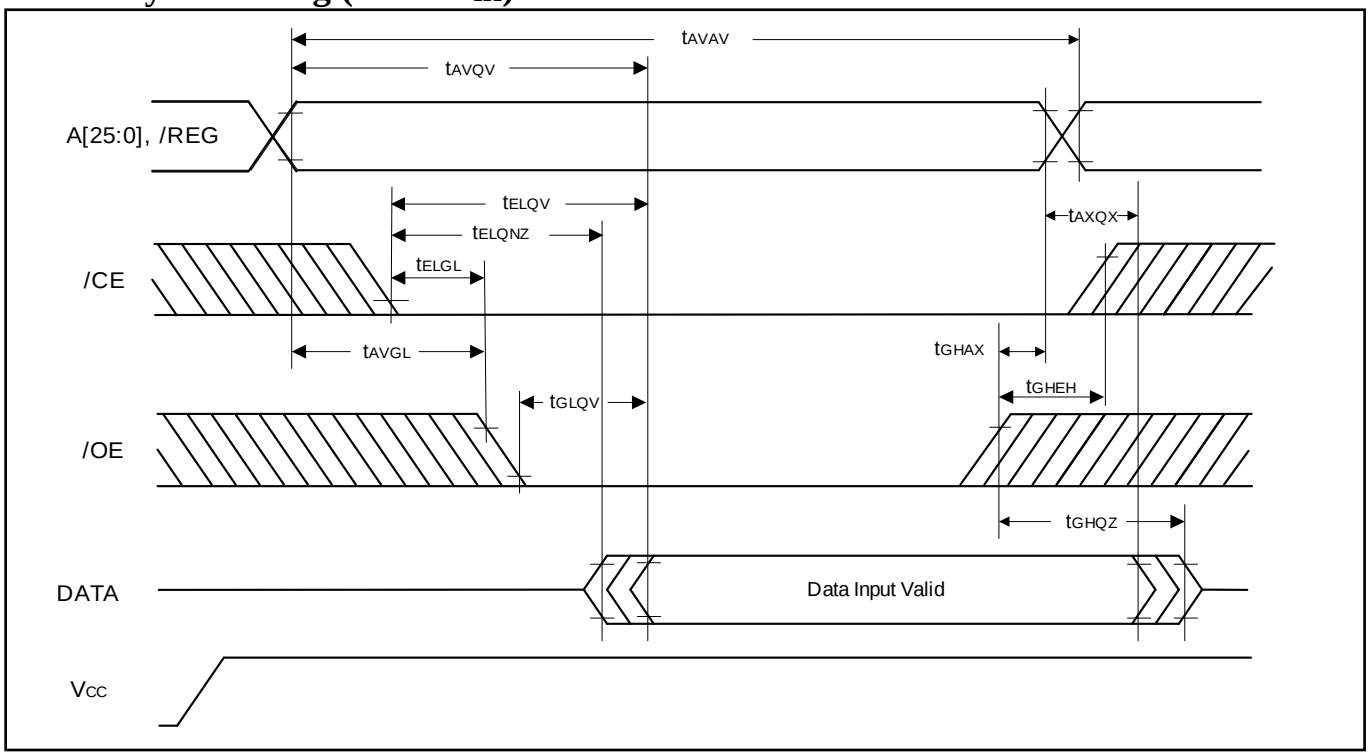
Write Cycle Timing (/OE = V_{HI})

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{AVAV}	150		ns
Write Pulse Width	t_{WLWH}	80		ns
Address Setup Time for /WE Low	t_{AVWL}	20		ns
Address Setup to /WE High	t_{AVWH}		100	ns
Card Enable Setup to /WE Low	t_{ELWH}	100		ns
Data Setup to /WE High	t_{DVWH}	50		ns
Data Hold from /WE High	t_{WHDX}	20		ns
Address Hold from /WE High	t_{WHAX}	20		ns
Data Output Disable Time form /WE Low	t_{WLQZ}		75	ns
Data Output Disable Time form /OE Low	t_{GHQZ}		75	ns
/WE High time to Data Output Enable	t_{WHQNZ}	5		ns
/OE Low time to Data Output Enable	t_{GLQNZ}	5		ns
/OE High to /WE Low Setup time	t_{GHWL}	10		ns
/WE High to /OE Low Hold time	t_{WHGL}	10		ns
/CE Low to /WE Low Setup time	t_{ELWL}	0		ns
/WE High to /CE High Hold time	t_{WHEH}	20		ns

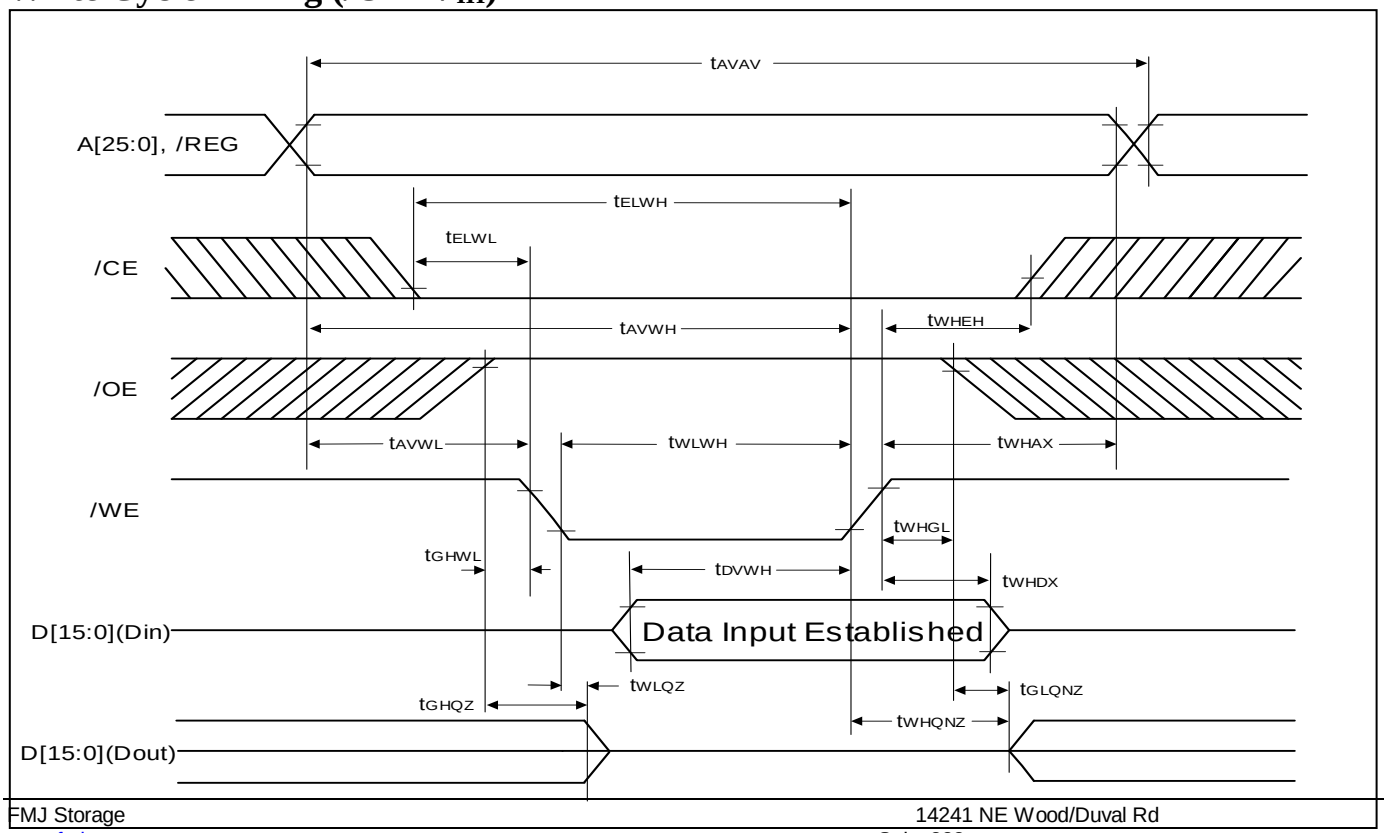
CARD TIMING CHARACTERISTICS *(CONTINUED)*

Common and Attribute Memory Read and Write Cycle Timing.

READ Cycle Timing (/WE=V_{IH})



Write Cycle Timing (/OE=V_{IH})

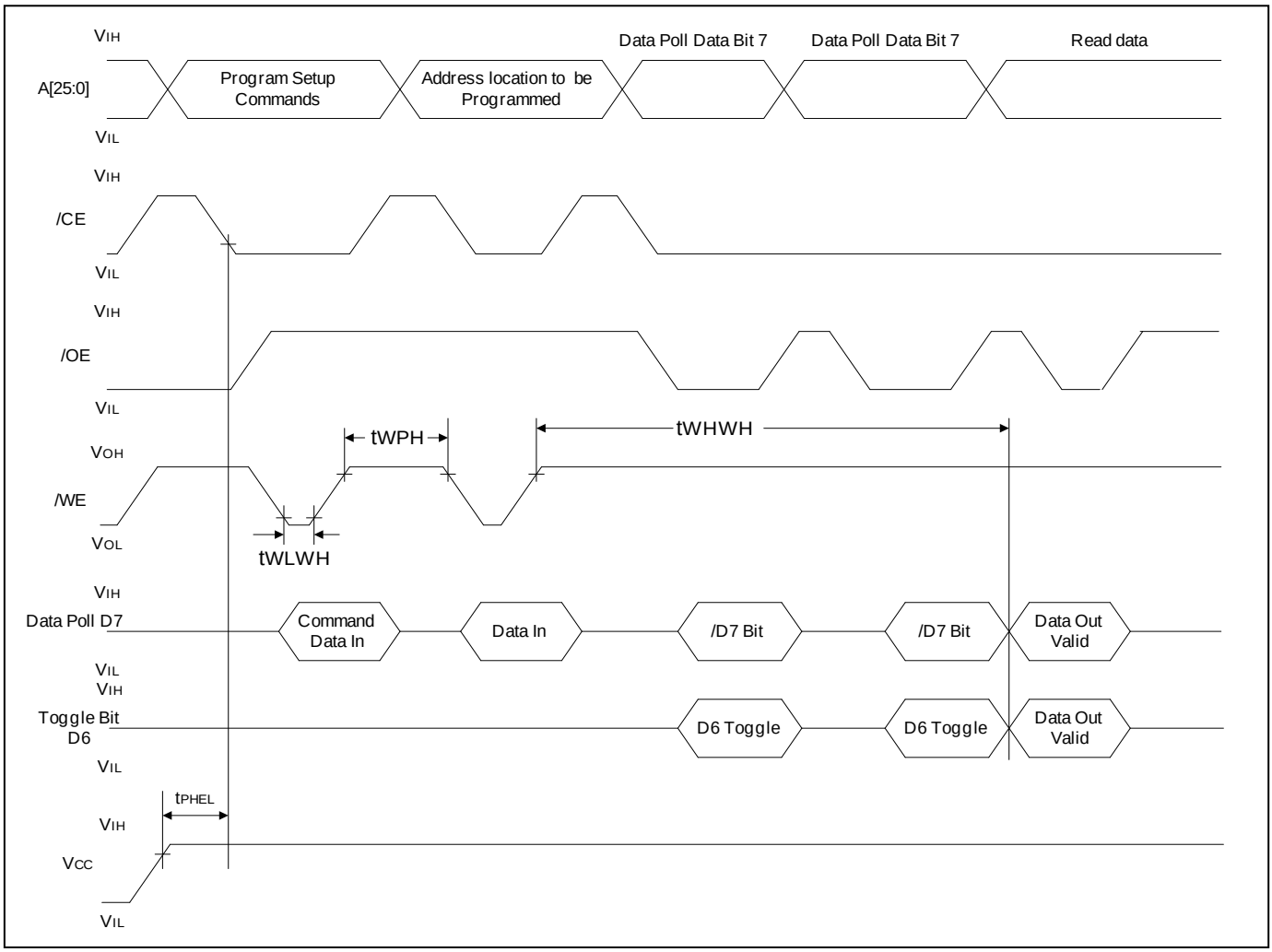


CARD TIMING CHARACTERISTICS *(NOTE 1)* *(CONTINUED)*

WRITE OPERATIONS AND DATA POLLING TIMING DIAGRAM

/WE controlled write timings and data polling.

Item	Symbol	Min	Typ	Max	Units
Power (VCC) High Recovery to /CE Going Low	t_{PHEL}	50			µs
Write Pulse Width	t_{WLWH}	80			ns
Write Pulse Width Hold High	t_{WPH}	85			ns
Chip Embedded Program Operations	t_{WHWH}		8		µs
				48	ms

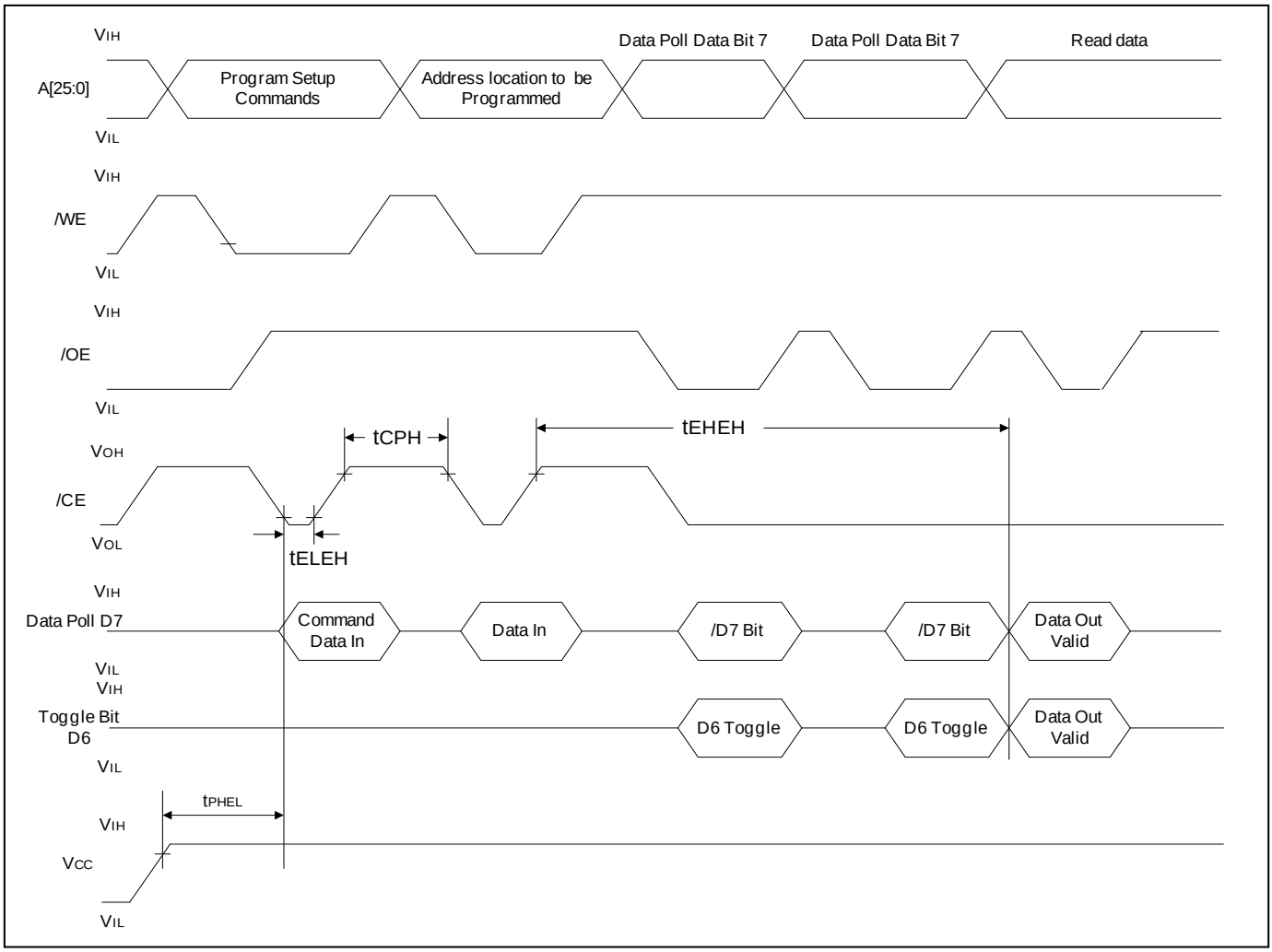


CARD TIMING CHARACTERISTICS *(CONTINUED)*

WRITE OPERATIONS AND DATA POLLING TIMING DIAGRAM

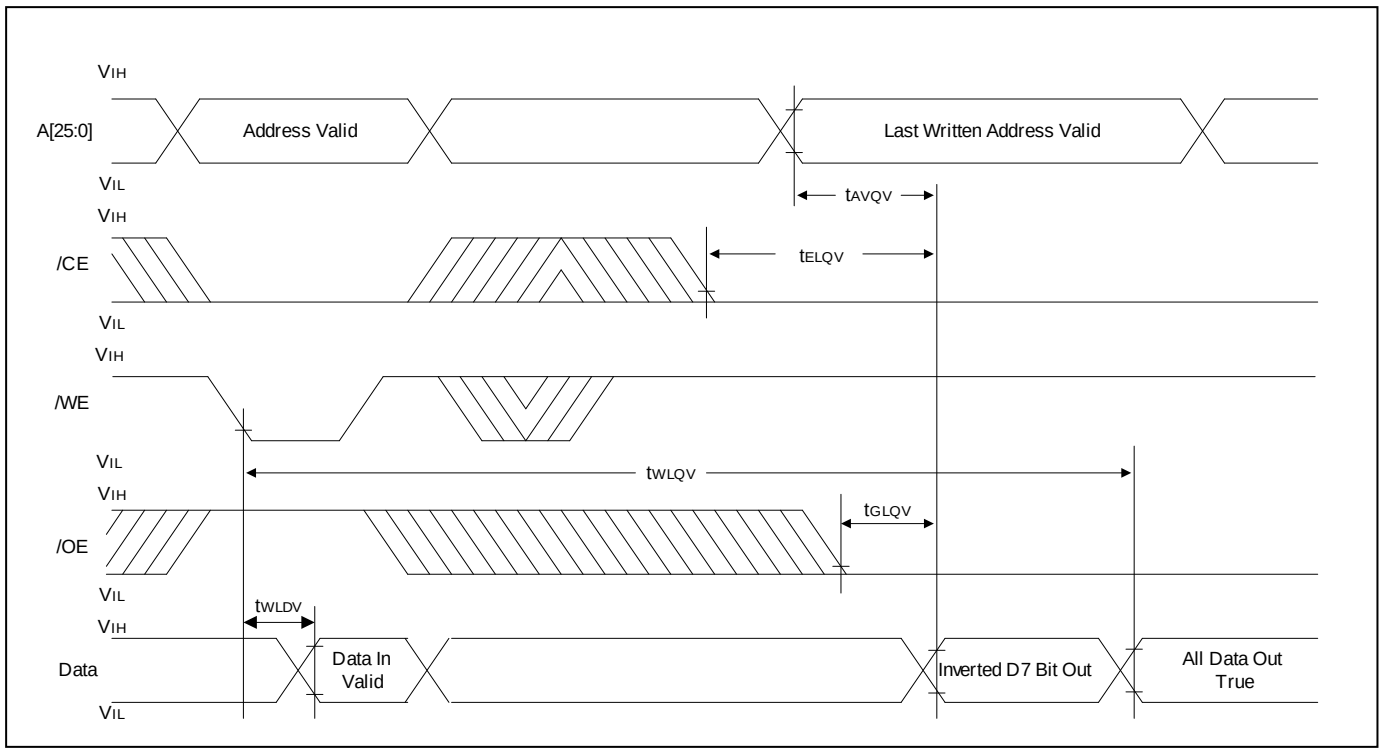
Alternate /CE controlled write timings and data polling

Item	Symbol	Min	Typ	Max	Units
Power (VCC) High Recovery to /CE Going Low	t_{PHEL}	50			µs
Enable Pulse Width	t_{ELEH}	65			ns
Enable Pulse Width Hold High	t_{CPH}	50			ns
Chip Embedded Program Operations **(Note 1, 2)**	t_{EHEH1}	16			µs
				48	ms
Chip Embedded Erase Operations for each 64K byte memory sector **(Note 3, 4)**	t_{EHEH2}	1.5			s



CARD TIMING CHARACTERISTICS *(CONTINUED)*

ATTRIBUTE MEMORY TIMING DIAGRAM



Attribute Parameter **(Note 1, 2)**	Symbol	**Min**	**Max**	**Unit**
Read Cycle Time	t_{AVAV}	200		ns
Card Enable Access Time	t_{ELQV}		200	ns
Output Enable Access Time	t_{GLQV}		70	ns
Write Enable Low to Data Valid Time	t_{WLDV}		1000	ns
Write Enable Low to Data Read Valid Time	t_{WLQV}		1	ms

Note:

1. *All timing values are constant with standard Read/Write Times, unless otherwise shown in the Table.*
2. *Attribute memory latches address values on the falling edge of /WE. Data is latched on the rising edge of /WE.*

Attribute Data Polling Mode:

Data Polling, the 28C16A features /DATA polling to signal the completion of a byte write cycle. During a write cycle, an attempt to read the last byte written to memory will produce the complement of the D7 (D6 to D0 are indeterminate). After completion the true data is available. Data Polling allows a simple read/compare operation to determine the status of the chip.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min.	Max.	Units
Vcc Supply Voltage	Vcc	4.75	5.25	V
Industrial Operating Temperature	T_A	-40	85	°C

DC CHARACTERISTICS

Supply current is an RMS value. Typical values at nominal V_{CC} voltage at T_A = +25°C.

Symbol	Parameter	Condition	Min	Max	Units
I_{CCS}	Standby Current **(Note 2)**	Per device: CMOS; V_{CC} = V_{CC} Max , V_{IN} = GND to V_{CC} /CE1, /CE2, = V_{CC} ±0.2V		100	µA
I_{CCR}	Active Read Current **(Note 1, 2)**	CMOS; V_{CC} = V_{CC} Max /CE1 or /CE2 = GND **Byte (×8)** I_{OUT} = 0mA, at f = 3.3MHZ		45	mA
		Byte (×16)		90	mA
I_{CCW}	Active Program Current **(Note 1, 3)**	Per device: /CE1 or /CE2 = GND (including programming current)		65	mA
I_{CCE}	Active Sector Erase Current **(Note 3)**	Per device: (including programming current)		65	mA
I_{IL}	Input Leakage Current	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin:		+20	µA
I_{ILpu}	Input Leakage Current with Pull Up Resistor	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin with 10KΩ pull up resistor		+500	µA
I_{ILpd}	Input Leakage Current with Pull Down Resistor	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin with 100KΩ pull down resistor		-50	µA
I_{OLpd}	Output Leakage Current with Pull Down Resistor	V_{OUT} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin with 100KΩ pull down resistor		±20	µA
V_{IL}	Input Low Voltage **(Note 3)**		-0.5	0.8	V
V_{IH}	Input High Voltage **(Note 3)**		0.7 × V_{CC}	V_{CC} +0.3	V
V_{OL}	Output Low Voltage **(Note 3)**	V_{CC} = V_{CC} Min I_{OL} = 3.22 mA		0.40	V
V_{OH}	Output High Voltage **(Note 3)**	CMOS; V_{CC} = V_{CC} Min I_{out} = 2.0 mA	3.8	V_{CC}	V
V_{LKO}	Low V_{CC} (Lock-Out)		3.2	4.2	V

Notes:

1. *I_{CCWS} and I_{CCES} are specified with the device deselected. If read or written while in erase suspend mode, the device's current is the sum of I_{CCWS} or I_{CCWS} and I_{CCR} or I_{CCW}.*
2. *CMOS inputs are either VCC ± 0.2V or GND ± 0.2V.*
3. *Sample tested by component manufacturer.*

CARD INFORMATION STRUCTURE

The CIS is data which describes the PCMCIA card and is described by the PCMCIA standard. This information can be used by the Host system to determine a number of things about the card that has been inserted. For information regarding the exact nature of this data, and how to design Host software to interpret it, refer to the PCMCIA standard Metaformat Specification.

Physical Address	Logical Address	Data Value(s)	Tuple Description
00h	00h	01h	CISTPL_DEVICE
02h	01h	03h	CISTPL_LINK
04h	02h	53h	Speed = 150ns, WPS=Yes, FLASH
06h	03h	**9Eh** ***(Note 1)***	Bits 2-0 = 110b = 2 Meg units, Bits 7-3 = 10011b = 20 Units (0=1, 1=2...) 2 Meg x 20 = 40 Meg size
08h	04h	FFh	CISTPL_END - End of Tuple
0Ah	05h	18h	CISTPL_JEDEC
0Ch	06h	03h	CISTPL_LINK
0Eh	07h	89h	Manufacturer ID (AMD)
10h	08h	ADh	Device ID (Am29F016)
12h	09h	FFh	CISTPL_END - End of Tuple
14h	0Ah	1Eh	CISTPL_DEVICEGEO
16h	0Bh	07h	CISTPL_LINK
18h	0Ch	02h	DGTPL_BUS - Bus Width - 2 Bytes
1Ah	0Dh	11h	DGTPL_EBS - Erase Block Size 2^10h = 64K Bytes or Words
1Ch	0Eh	01h	DGTPL_RBS - Byte Accessible
1Eh	0Fh	01h	DGTPL_WBS - Byte Accessible
20h	10h	01h	DGTPL_PART - One Partition
22h	11h	01h	DGTPL_HWIL - No Interleave
24h	12h	FFh	CISTPL_END - End of Tuple

CARD INFORMATION STRUCTURE *(CONTINUED*

Physical Address	Logical Address	Data Value(s)	Tuple Description
26h	13h	15h	CISTPL_VERS1
28h	14h	55h	CISTPL_LINK
2Ah	15h	04h	TPLLV1_MAJOR (PCMCIA 2.1/JEIDA 4.2)
2Ch	16h	01h	TPLLV1_MINOR
2Eh...66h	17h...33h	46 4d 4a 20 53 74 6f 72 61 67 65 2c 20 69 6e 63 2e	ASCII Text is : FMJ Storage, Inc. {17 Characters total}
68h	34h	00	NULL String Delimiter (String 1)
6Ah...84h	35h...42h	46 4C 34 30 4D 2D 31 35 2D 32 31 31 31 39	ASCII Text is : ***(Note 2)*** {14 Characters total}
86h	43h	00	NULL String Delimiter (String 2)
88h...CCh	44h...66h	33 32 20 4d 45 47 20 46 4c 41 53 48 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20	ASCII Text is : ***(Note 3)*** **32 MEG FLASH** {34 Characters total}
CEh	67h	00	NULL String Delimiter (String 3)
D0h	68h	00	NULL String Delimiter (String 4)
D2h	69h	FF	CISTPL_END - End of Tuple

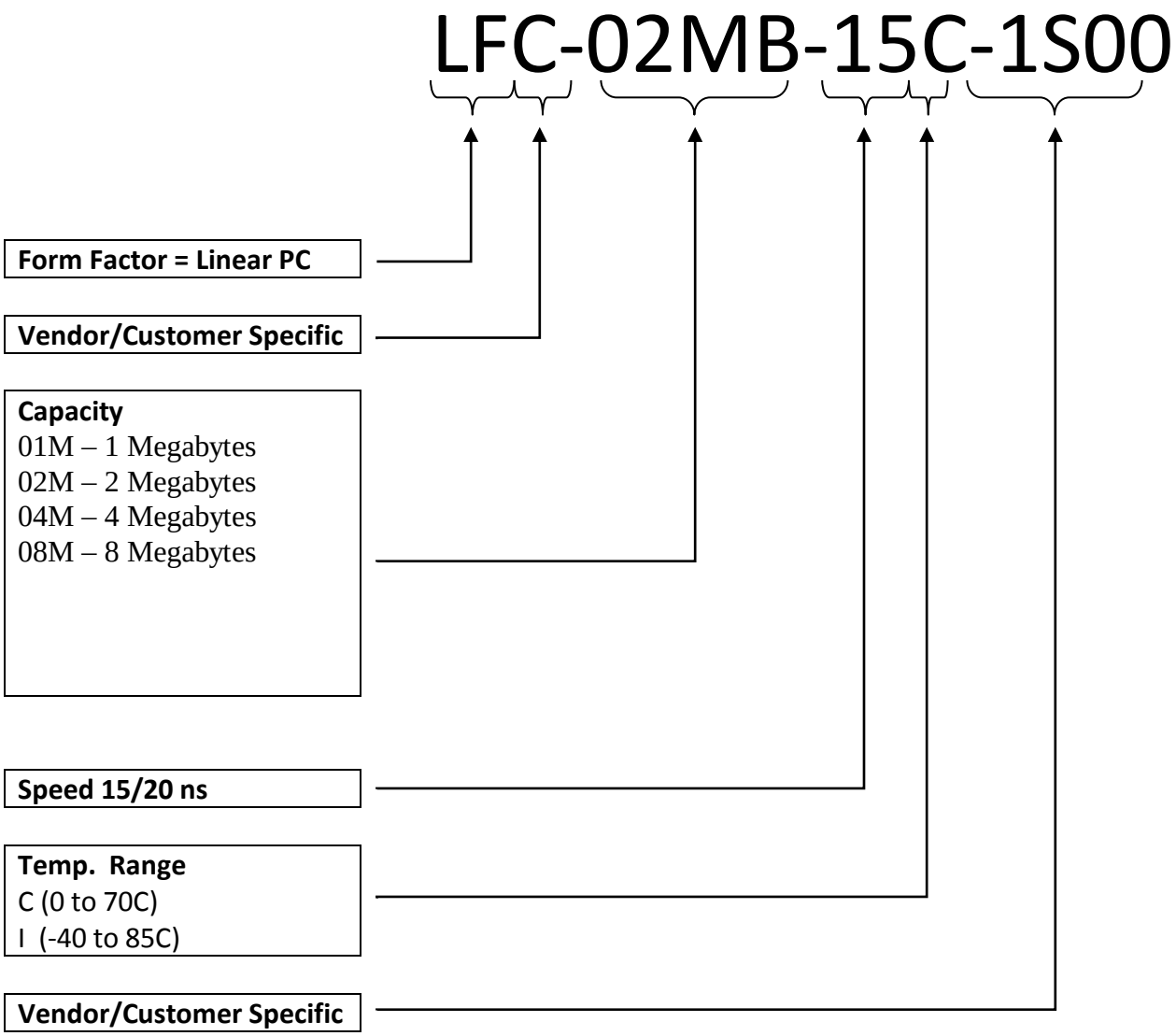
D4h	6Ah	FF	CISTPL_END - End of Chain Tuple

Notes:

2. *Specific Product description will be listed (See Note 1 Part Numbers).*
3. *Specific Product memory capacities will be listed for specific products.*

ORDERING INFORMATION

The following describes the part number ordering nomenclature from FMJ Storage.



- Available In Type II PCMCIA only